

REMARKS

Claims 1-9 are pending in the application. These claims were rejected as follows:

| Claims / Section | 35 U.S.C. Sec. | References / Notes |
|------------------|---------------------|--|
| 1, 2, 4-6, 8 & 9 | §102(b) Obviousness | <ul style="list-style-type: none">Furuhata (U.S. Patent No. 5,521,421). |
| 3,7 | §103(a) Obviousness | <ul style="list-style-type: none">Furuhata (U.S. Patent No. 5,521,421); andRoth, Fundamentals of Logic Design (1992). |

- 5 Applicant responds with the following arguments distinguishing the present invention from the art cited against it.

35 U.S.C. §102(b), CLAIMS 1, 2, 4-6, 8 & 9 ANTICIPATION BY FURUHATA

1. *Furuhata fails to teach each and every element of the present invention because it fails to describe a charge carrier detector element,*
10 *according to the present invention.*

In the OA, under numbered paragraph 2, the Examiner indicates that Furahata discloses a charge carrier detector, referring to the PN junction of the region 14a and 13, according to Figures 1a-1b. According to claim 1 of the present invention, a charge carrier detector generates a second signal given the
15 occurrence of free charge carriers in the semiconductor body.

Referring to Figures 1a and 1b of Furuhata, these figures describe a semiconductor device including a power MOSFET and a temperature monitor element. The power MOSFET includes a plurality of cells connected in parallel. Each of these cells comprises a body-zone 14a, 14b disposed in a

semiconductor body 13 and are complementarily doped to the semiconductor body 13. These cells furthermore include source-zones 15a, 15b that are complementarily doped to the body-zones 14a, 14b and gate-electrodes 16a, 16b for controlling a current path between the source-zones 15a, 15b and parts
5 of the semiconductor body 13, with the latter serving as the drift zone of the power MOSFET.

However, Furuhashi does not describe a charge carrier detector that generates a second signal given the occurrence of free charge carriers in the semiconductor body. The Examiner incorrectly equates the PN junction between
10 semiconductor regions 14a and 13 as such a charge carrier detector. Semiconductor zone 14a is part of the body zone of the power MOSFET and, together with source zone 15a, is connected to source electrode 17. The semiconductor body 13 and body zone 14a are part of the reverse diode of the power MOSFET. By applying a positive voltage between source electrode 17 and a drain
15 electrode (not depicted in Furuhashi) being connected to semiconductor body 13, this reverse diode allows a current to flow between source and drain electrode. The Examiner has failed to indicate how his construction of a charge carrier detector as construed by the PN junction of the region 14a and 13 generates a second signal given the occurrence of free charge carriers in the semiconductor
20 body. The purpose of the charge carrier detector and the appertaining signal generated by it is to prevent false positive indications by the temperature sensor. Furuhashi is completely devoid of any teaching relating to a second signal that is used in this manner.

2. *Furuhata fails to teach each and every element of the present invention because it fails to describe a temperature sensor integrated into the semiconductor body.*

According to claim 1 of the present invention, the temperature sensor is
5 integrated in the semiconductor body.

The semiconductor device according to Furuhata includes a temperature monitor element 18 that is disposed above a surface of the semiconductor body 13 and is electrically insulated from the semiconductor body 13 by insulating layer 19. Thus, Furuhata fails to teach this element of the present invention

10 For these reasons, Applicant believes that claim 1 and all remaining claims that depend therefrom are not anticipated by Furuhata and respectfully request that the 35 U.S.C. §102 rejection be withdrawn from the present application.

35 U.S.C. §103(a), CLAIMS 3 AND 7 OBVIOUSNESS OVER FURUHATA IN VIEW OF ROTH

15 3. *Applicant relies on the arguments provided under numbered paragraphs 1 and 2 above and assert that the addition of Roth does not obviate claim 1 of the present invention.*

Applicant relies on the above arguments indicating that Furuhata does not teach or suggest the charge carrier detector generating a second signal or the
20 temperature sensor being located in the semiconductor body. The Examiner combines Roth for the teaching of the use of an exclusive-or logic gate, and thus does not provide it as teaching these missing elements. Of note, the Examiner does not provide any indication of how this evaluation mechanism would be

connected to the first and second signals (particularly in the absence of a second signal) or integrated with the semiconductor switch.

For these reasons, the Applicant asserts that the claim language clearly distinguishes over the prior art, and respectfully request that the Examiner
5 withdraw the §103(a) rejection from the present application.

CONCLUSION

Inasmuch as each of the objections have been overcome by the amendments, and all of the Examiner's suggestions and requirements have been satisfied, it is respectfully requested that the present application be reconsidered,
10 the rejections be withdrawn and that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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25 I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on September 5, 2003.

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